

G. 1A

A cross-sectional view of a device structure 100. The structure features a central rectangular region 52 with diagonal hatching. This central region is flanked by two side regions 44, also with diagonal hatching. The side regions 44 are separated from the central region 52 by narrow gaps 42. The top and bottom surfaces of the central region 52 are defined by layers 52b. The top surface of the central region 52 is also defined by a layer 11. The bottom surface of the central region 52 is defined by a layer 20. The width of the central region 52 is indicated as 2.5 μm, and the width of the side regions 44 is indicated as 1 μm. A dashed line A-A indicates the plane of the cross-section.

FIG. 1B is a cross-sectional view of a semiconductor device. The device is built on a substrate 10. A base layer 12 is formed on the substrate. A central region 20 contains a gate stack 18/16 and a channel 22. The device is flanked by source/drain regions 30/40. A top layer 50 is shown with a patterned layer 52a. Various other layers and structures are labeled with numbers 14, 24, 26, 28, 32, 34, 36, 38, 42, 44, 46, 48, and 50.

2/11

FIG. 2A

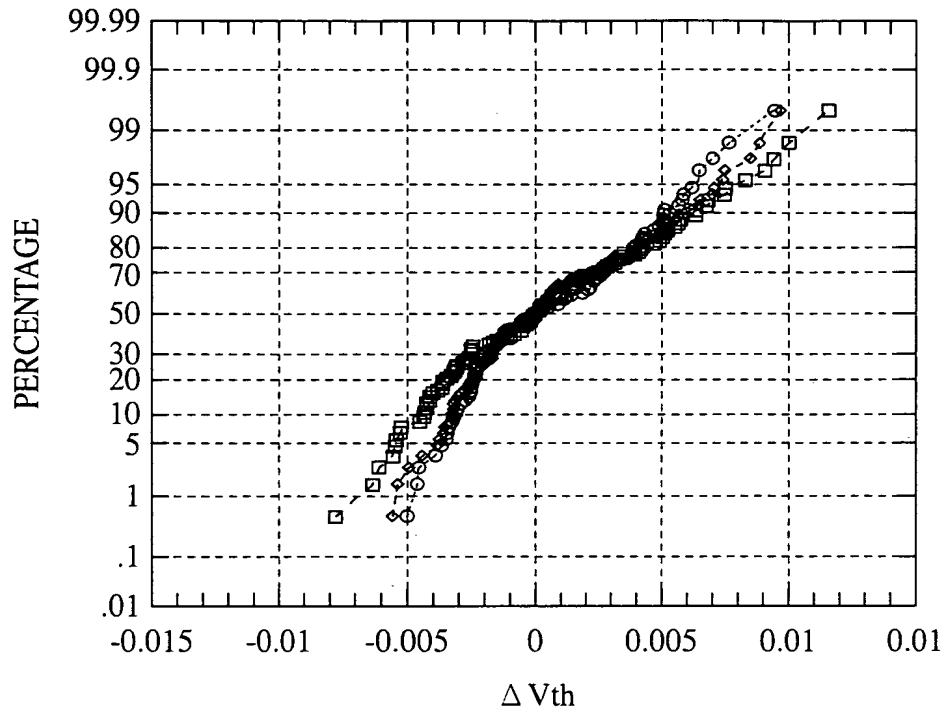


FIG. 2B

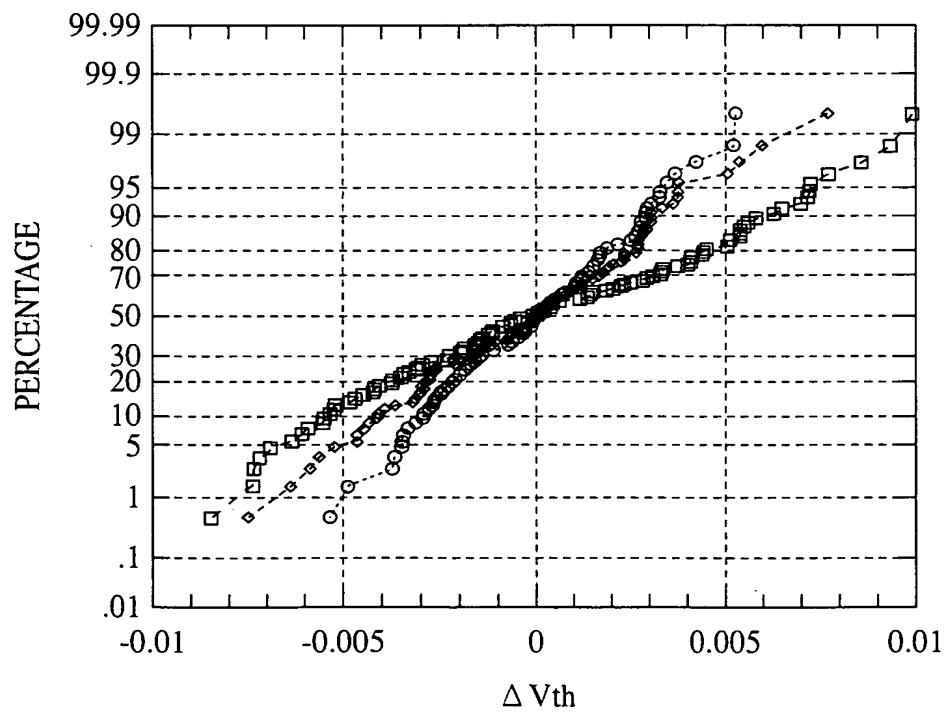
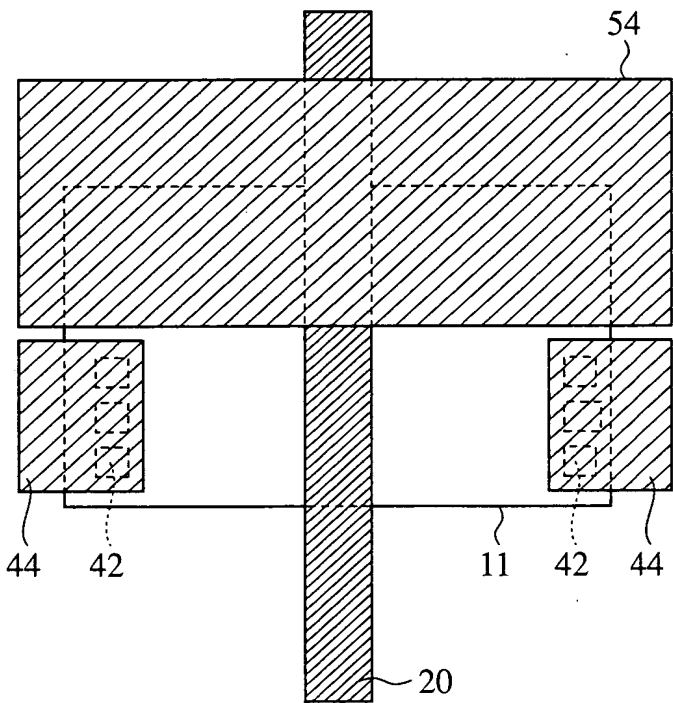
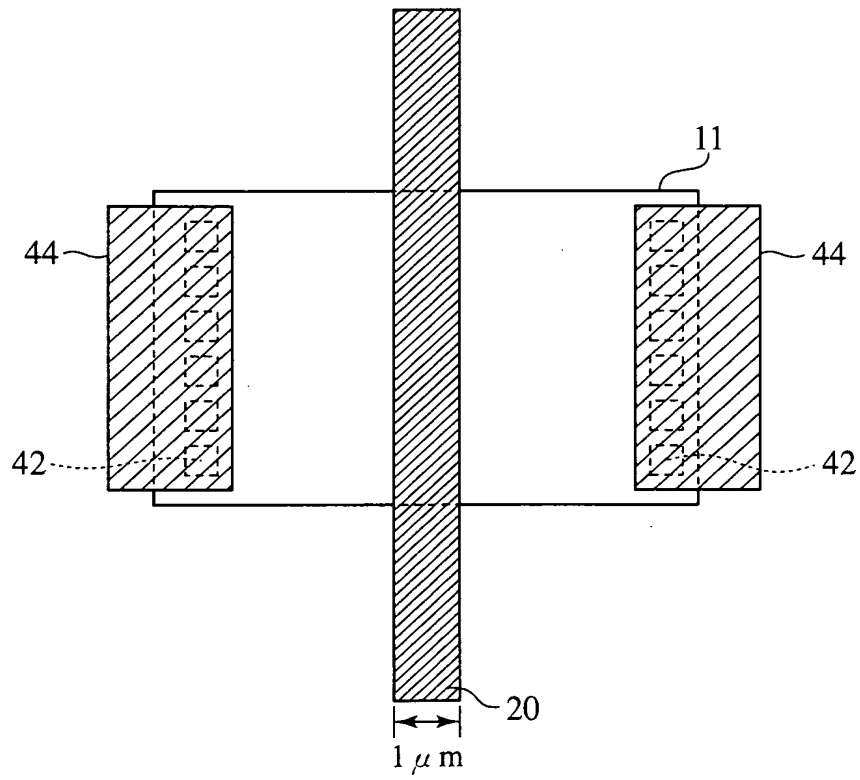


FIG. 3



4/11

FIG. 4



5/11

FIG. 5A

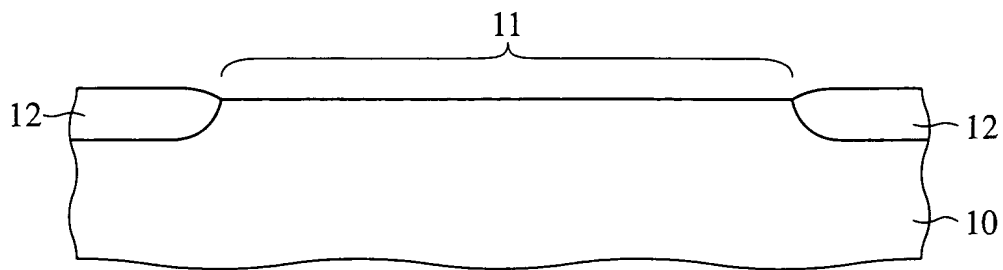


FIG. 5B

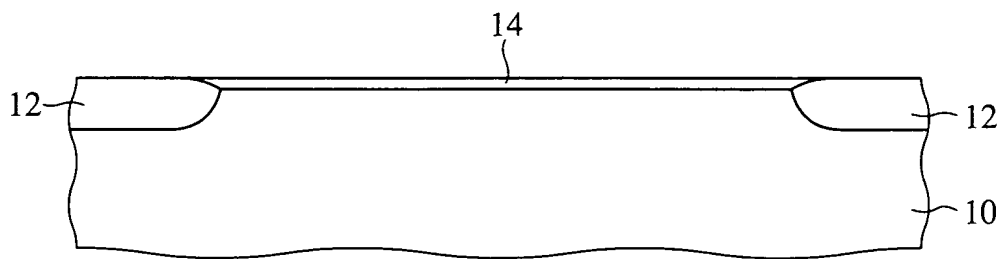
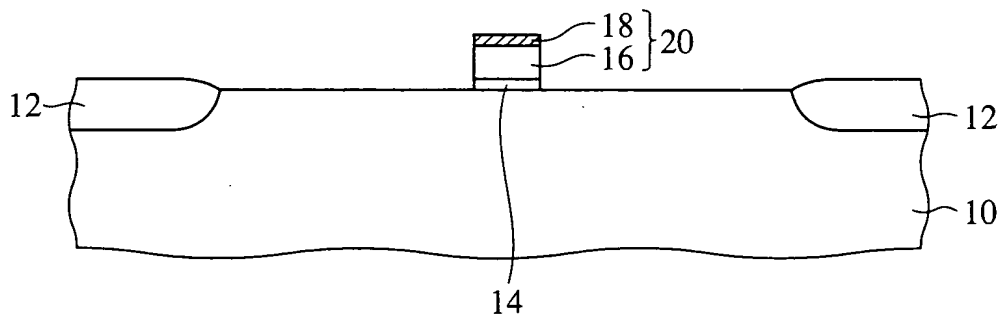


FIG. 5C



6/11

FIG. 6A

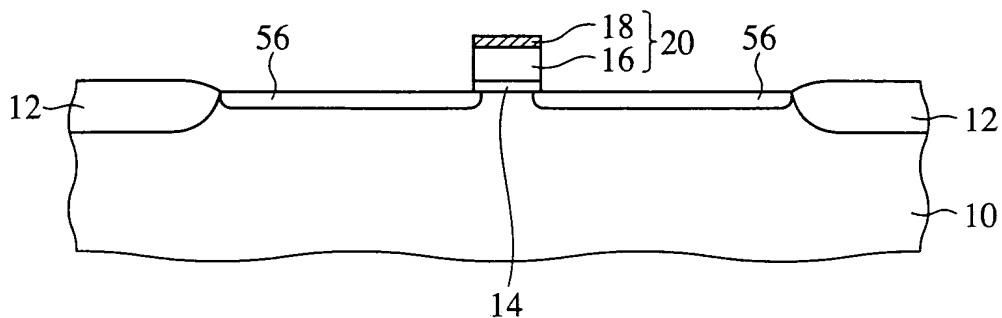


FIG. 6B

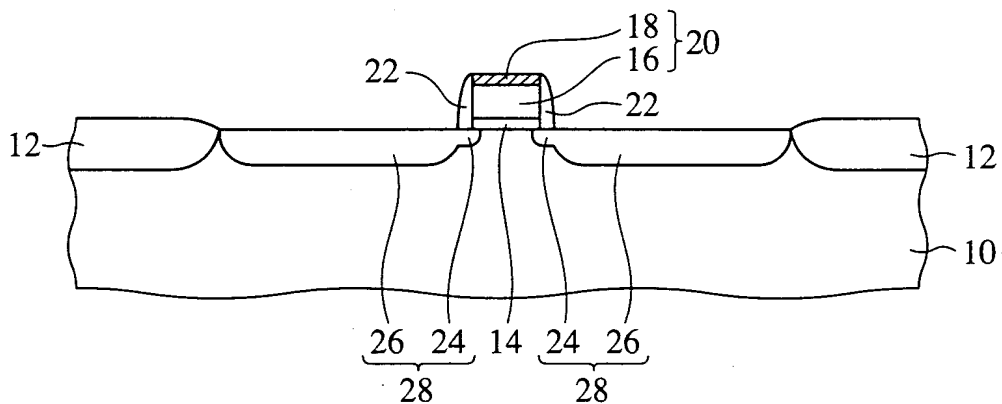
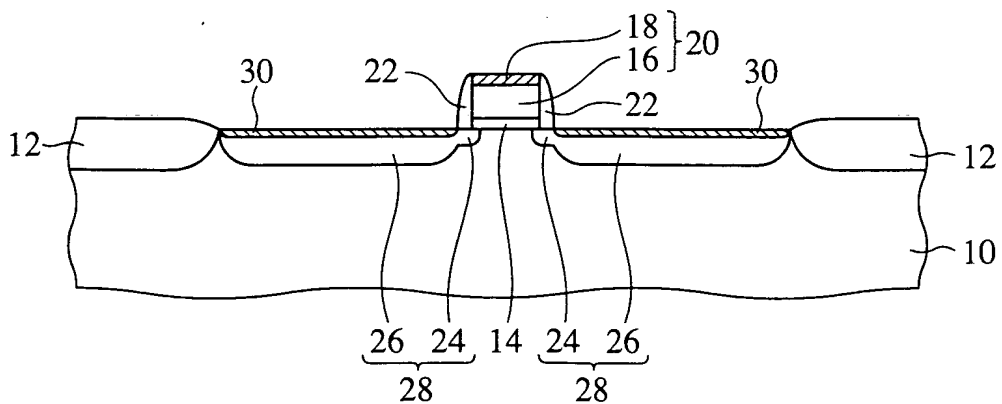


FIG. 6C



7/11

FIG. 7A

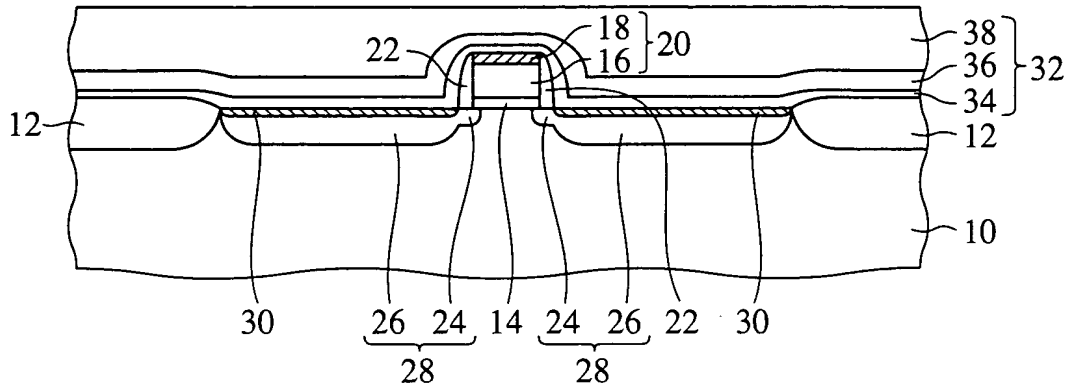


FIG. 7B

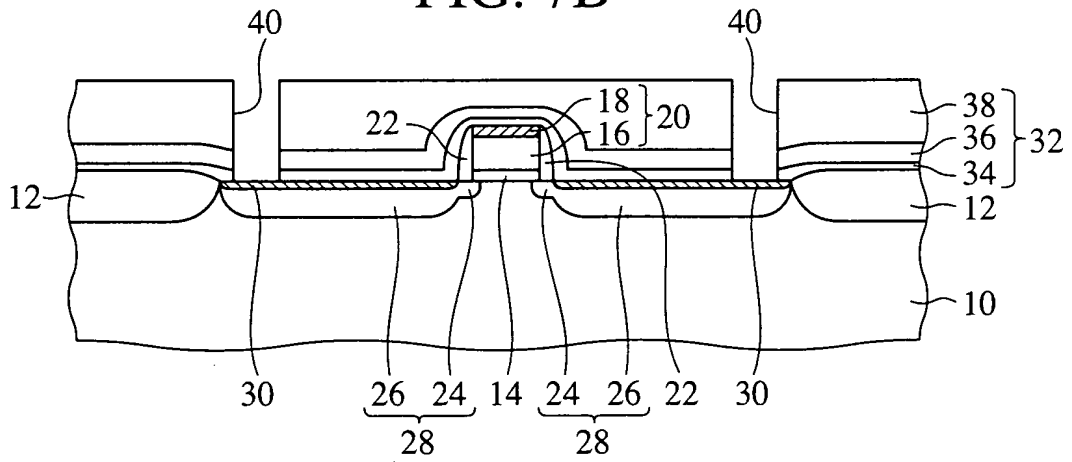
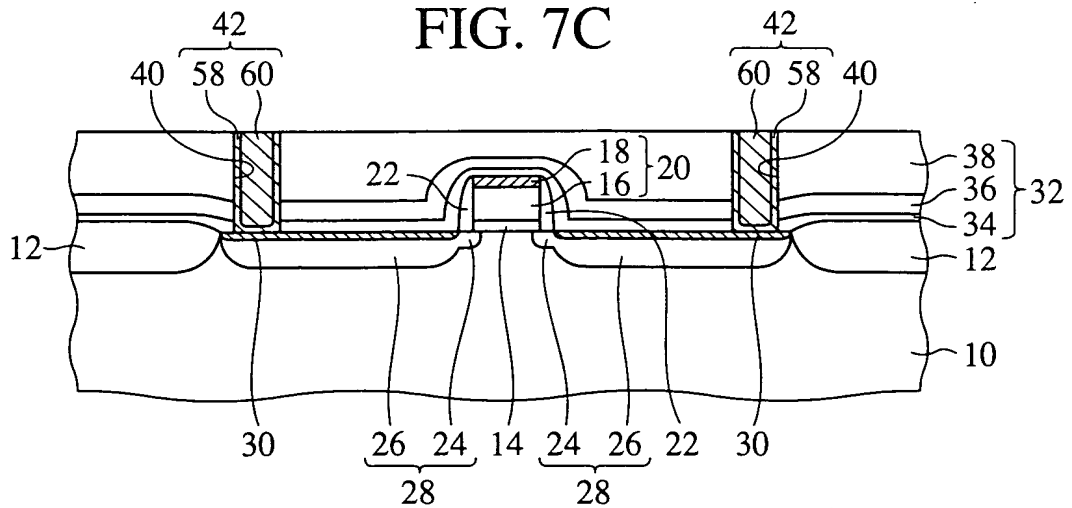


FIG. 7C



8/11

FIG. 8A

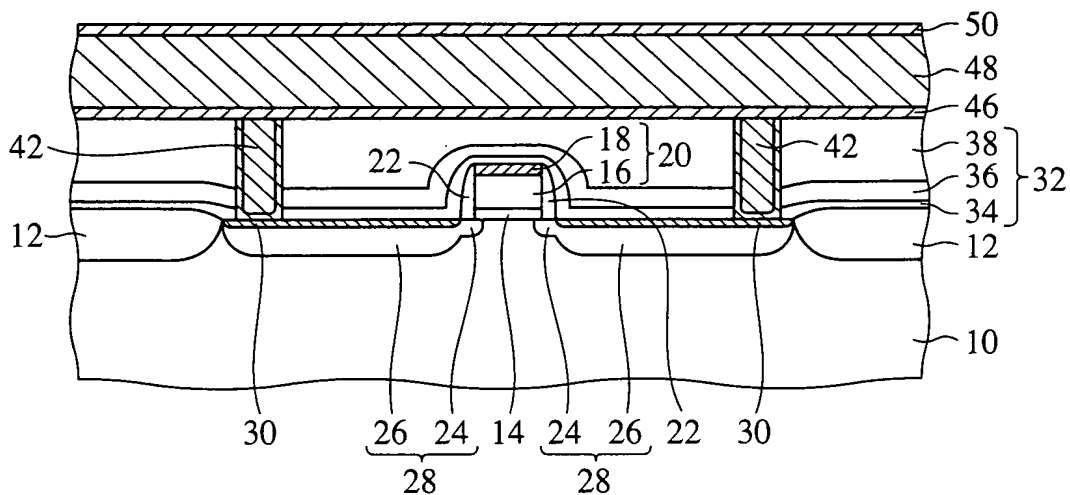
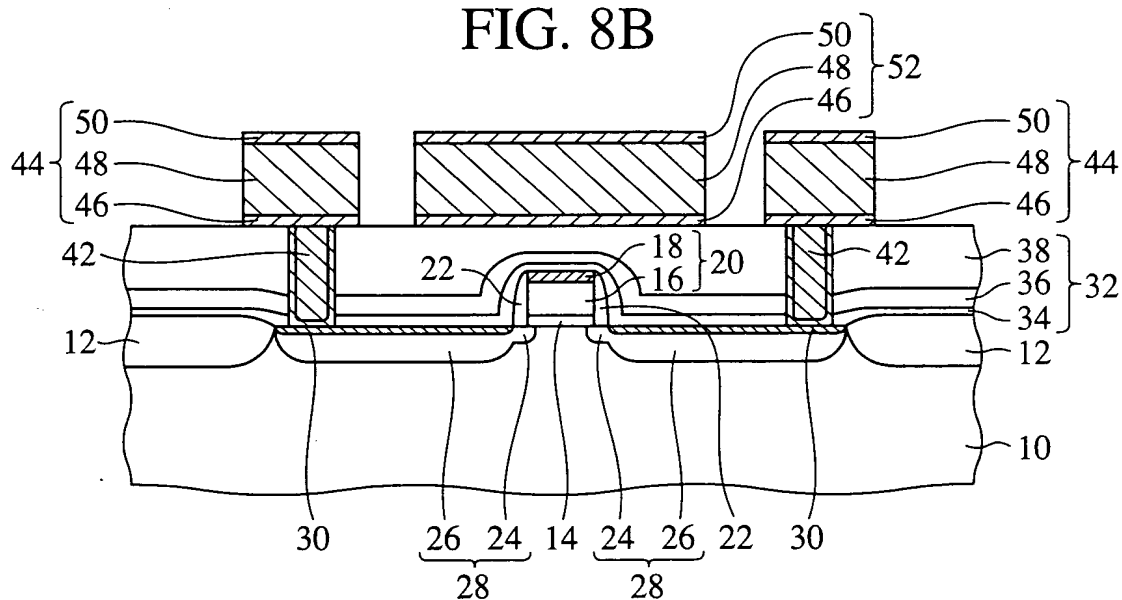
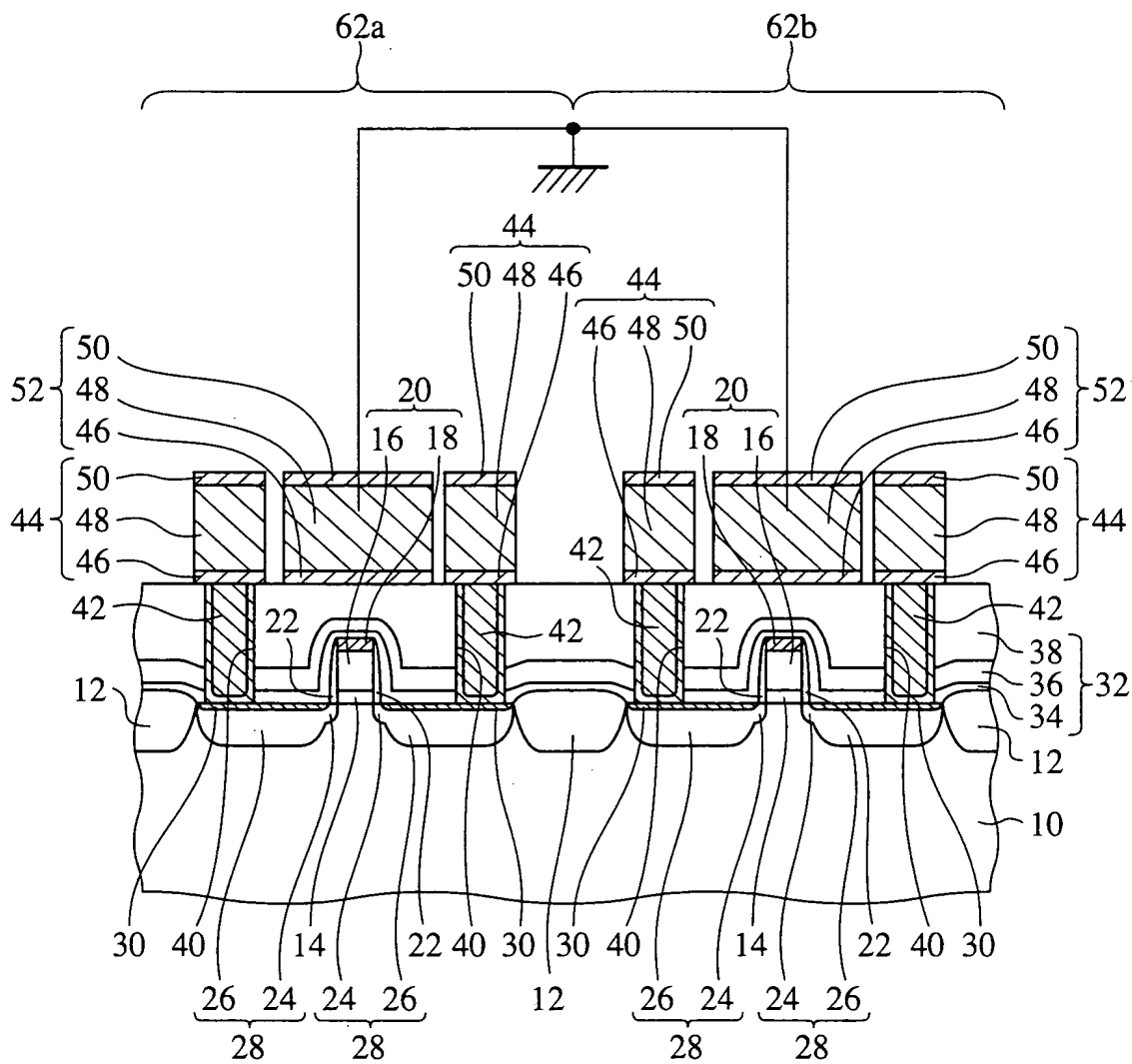


FIG. 8B







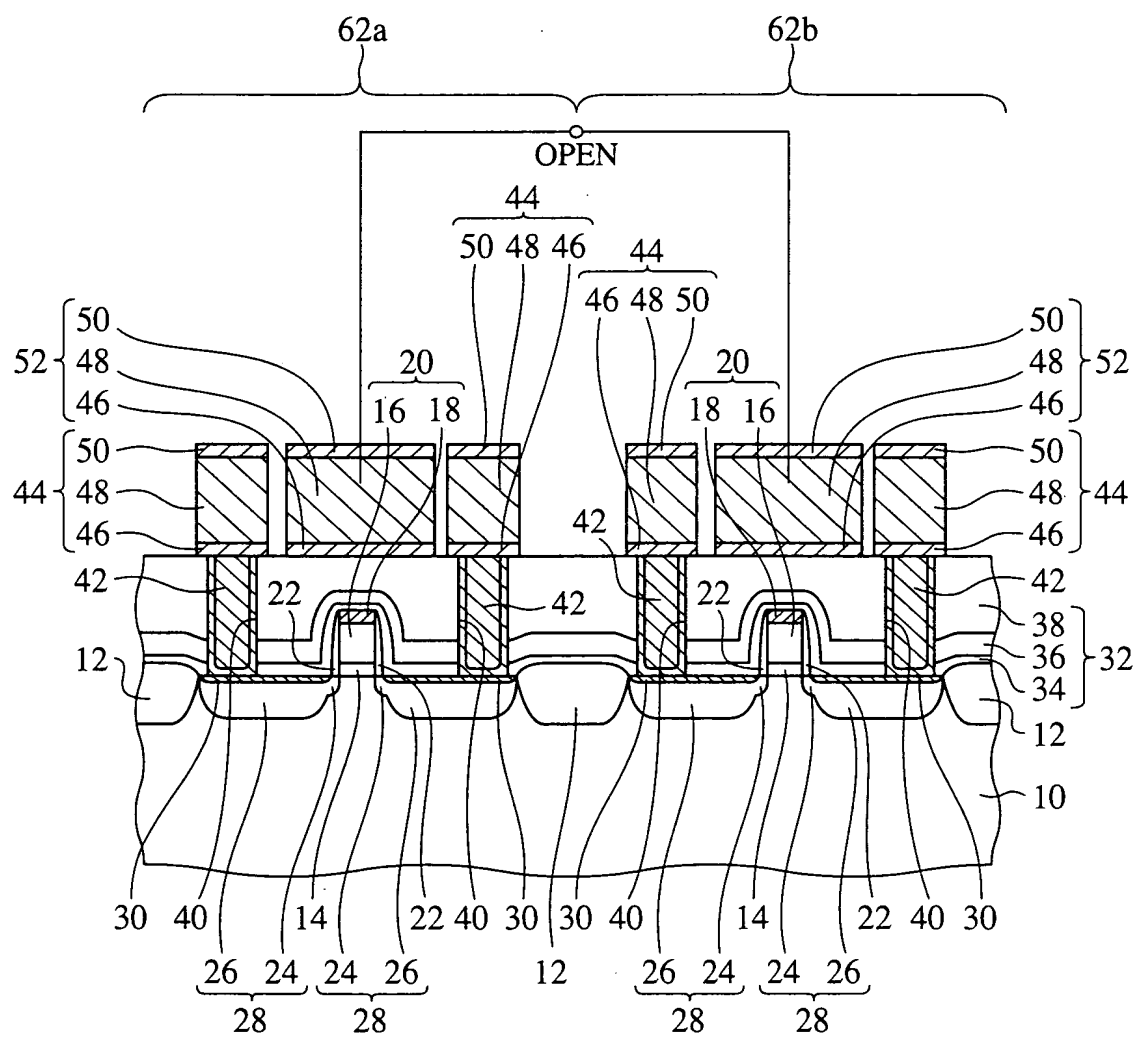


FIG. 11

